Exhibit D

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORP.
Requester 1,

SMART MODULAR TECHNOLOGIES, INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2018-003618
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/000,579
Patent No. 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION UNDER 37 C.F.R. § 41.77(f)

STATEMENT OF THE CASE

These proceedings involve U.S. Patent No. 7,619,912 B2 ("the '912 patent), issued November 17, 2009 to Jayesh R. Bhakta and Jeffrey C. Solomon.

In our earlier Decision ("Dec.") mailed May 31, 2016, we affirmed the Examiner's decision not to reject: (1) claims 1, 3, 4, 6, 10, 11, 14, 15, 18–20, 24, 25, 28, 29, 31, 32, 34, 36, 37, 39–43, and 46 based on Amidi[1] under § 102, (2) claims 1, 3, 4, 6, 10–20, 24, 25, 27–29, 31, 32, 34, 36–43, 45–48, 50, 52–54, 56, 58, 67–71, 75, 77–89, 92, 93, 120–126, 128–130, 132, 133, and 135 based on Amidi under § 103, (3) claims 56, 60–63, 90, 91, 109–111, 127, and 131 based on Amidi and JEDEC[2] under § 103, (4) claims 16 and 17 based on Amidi and Dell 2[3] under § 103, and (5) claims 57,[4] 58, 60, 68, 79, 84, 89–91, and 128–131 under § 112, first paragraph, as lacking written description support. Dec. 101–02. We additionally reversed the Examiner's decision not to adopt the rejections of:

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[1] U.S. Publ. 2006/0117152 A1 (published June 1, 2006 and filed Jan. 5, 2004) (Amidi).

[2] JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C); *JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C* (Rev. of JESD79B) 1-75 (Mar. 2003) (JEDEC 79C); *JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A)* 1-12 (May 2003) (JEDEC 82-4B). As indicated in the previous Decision, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

[3] U.S. Patent No. 6,209,074 (issued Mar. 27, 2001) (Dell 2).

[4] The summary at the end of the Decision (Dec. 102) mistakenly omits independent claim 57. *See id.* at 84–89 (discussing claim 57 under the Lack of Written Description Support section).

III. ANALYSIS

A. Amidi and Dell 2 (Ground 5)

In our May 31, 2016 Decision, claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 (canceled claims omitted) were rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 78–83. Patent Owner presents several argument related to this ground, asserting the amendments to independent claims 1, 15, 28, and 39 overcome the new grounds. PO Response 50–53. Patent Owner asserts the claimed "logic element [now] generates certain output control signals (e.g., gated column access strobe (CAS) signals or chip-select signals recited in claim 1) in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and [sic] (iii) the at least one chip-select signal of the set of input control signals, and (iv) the PLL [phase lock loop] clock signal." *Id.* at 52; *see also id.* at 3 (underlining omitted). Throughout this Decision, we will refer to this new limitation as the "logic element" limitation and the response signals collectively as signals (i)–(iv) or individually as signal (i), (ii), (iii), or (iv).

Regarding the "logic element" limitation, Patent Owner argues (1) "Amidi's CPLD 604 never receives bank address signals," instead generating control signals (e.g., chip select signals rcs0a–rcs3b) based on a row address signal and chip-select signals and (2) Dell 2 does not cure Amidi's deficiencies. *Id.* at 52 (citing 2d Supp. Sechen Dec. ¶¶ 21–22, 25). Additionally, Patent Owner argues combining Amidi and Dell 2 would not teach or suggest to one skilled in the art generating control signals based on a row address signal and bank address signals as now recited in the claims. *See id.* at 52–53 (citing 2d Supp. Sechen Dec. ¶¶ 23–24, 26).

The Examiner maintained the Amidi/Dell 2 rejection on remand. Ex. Deter. 21. Citing to Requester 1–3's Comments, the Examiner determined the newly amended claim recitations, including the "logic element" limitation, have already been rejected in our previous Decision when addressing then existing claims 123, 128, and 129 (claims 128 and 129 are now canceled). *Id.* at 18 (citing R1 Comments 9, R2 Comments, and R3 Comments). Specifically, Requester 1 contends our previous Decision already determined Amidi and Dell 2 teach the recited "logic element" limitation. R1 Comments 7, 10–11 (citing 4th Wang Decl. ¶ 26 and Dec. 80–82, which refer to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach" (*id.* at 81)); *see also id.* at 40–43 (citing Amidi ¶ 71, Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1, and 3d Bagherzadeh Decl. ¶ 37), 57–60 (citing Dell 2, 2:48–59, 8:36–41), 78–79 (citing Dell 2, 2:32–38). Requesters 2 and 3 present similar remarks. *See* R2 Comments 8–9 (discussing the similarities of the new claim amendments to claims 52, 123 (previously existed),[13] and 129 (now canceled)); *see also* R3 Comments 7–8 (discussing the previously existing claim 123).

We agree independent claim 52 and claim 123 (previously recited) included a recitation similar to the "logic element" limitation. For example, claim 52 previously recited "the logic element responds to at least a row address bit of the at least one row/column address signal, the bank address signals, and the at least one

[13] Requester 2 cites to "RAN Claims 42." R2 Comments 8. Requester 2 states "RAN Claims" refers to "Patent Owner Response/Amendment" submitted on January 14, 2013. *Id.* at 1. Because the amendment to claim 123 is located on page 38 (RAN Claims 38), we presume Requester 2 is referring to page 38 in the comments.

chip-select signal by generating a first number of chip-select signals of the set of output control signals." R1 App. Br., App'x A 17 (Claims App'x). Dependent claim 123 depends from claim 1 and previously recited "the logic element is responsive at least in part to a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select signals of the set of output control signals." *Id.*, App'x A 27 (Claims App'x). That is, other than the additional signal (iv) or the PLL clock signal now in claim 1 (PO Response 3), claim 1's "logic element" limitation generates chip-select signals in response to the same signals listed in previously recited claims 52 and 123.

However, when addressing Ground 5 (i.e., Amidi and Dell 2), we did not present a new ground of rejection for claim 52, 123, or 129. Dec. 78–83. Rather, we only presented a new ground of rejection for claims 52, 123, and 129 collectively based on Micron and Amidi (Ground 13). Dec. 93–99. As such, although these claims include similar subject matter to claim 1 as currently amended, we did not previously determine Amidi and Dell 2 teach or suggest the limitations found in claims 52, 123, and 129. Moreover, claim 1 previously recited the logic element "generates gated column access strobe (CAS) signals or chip-select signals . . . in response at least in part to a bank address signal" (R1 App. Br., App'x A 1) but did not recite that the CAS signals or chip-select signals were in response to bank address signal*s* as well as signals (i), (iii), and (iv) as now recited in claim 1.

For reasons discussed below and based on the record, we agree with Patent Owner that Amidi and Dell 2 would not teach or suggest to an ordinarily skilled

artisan the "logic element" limitation, which claims the logic element generates chip-select signals[14] in response to all four enumerated signals (i)–(iv) in claim 1.

In our previous decision, a register (e.g., 408) and a CPLD (e.g., 604) collectively were mapped to the recited "logic element." Dec. 18 (stating "we also do not find the Examiner erred in further mapping CPLD 410 in combination with register 408 to the separately recited 'logic element.'") We analyzed whether Amidi taught or suggested a register (e.g., 408) receiving bank address signals. *See, e.g.*, Dec. 18–21, 27–34. As part of that analysis, we concluded Amidi at least suggests to an ordinarily skilled artisan some embodiments where signals other than those explicitly disclosed, including bank address signals, may be received by register 408. *See, e.g.*, Dec. 28, 30, 33.

However, as now claimed, claim 1 recites the logic element "generates chip-select signals" in response to signals (i)–(iv). In Amidi, its CPLD (e.g., 604 in Figures 6A-B)—not its registers—generates chip-select signals (e.g., rcs0a–3b). Amidi, Figs. 6A–B. Because Amidi's registers (e.g., 408, 418, and 608) do not teach or suggest "generat[ing] chip-select signals" (e.g., rcs0a–3b) and the signals Amidi's registers received do not attribute to the generated chip-select signals at Amidi's CPLD (*see* Amidi, Figs. 6A–B), Amidi's register (e.g., 408) can no longer be a component of claim 1's "logic element" limitation that generates the recited "chip-select signals" in response to signals (i)–(iv).

Amidi shows chip-select signals[15] (e.g., rcs0a–rcs3b) generated by CPLD 604 (e.g., a logic element). Amidi ¶¶ 52, 60, Figs. 6A–B. Also, Amidi teaches and

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[14] We discuss the alternatively generated, "gated column access strobe (CAS) signals" of claim 1 later in the Opinion.
[15] The '912 patent explains "rank-select signals" are "also called chip-select signals." The '912 patent 2:36–38.

shows a row address signal (e.g., Add(n) or signal (i)) and a chip-select signal (e.g., cs0 or cs1 or signal (iii)) are inputted into Amidi's CPLD 604. Amidi ¶¶ 49, 52, 58, 60, Fig. 6A. As such, Amidi generates chip-select signals in response to both signals (i) and (iii) in claim 1. But, as we previously found, Amidi "fails to describe or show in Figures 4A–B and 6A–B a bank address signal entering CPLD 410 or 604. *See* Amidi, Figs. 4A–B, 6A–B." Dec. 20; *see id.* at 36. Additionally, we agreed with Patent Owner that "Requester 1's proposed obviousness rejections based on Amidi or Amidi and JEDEC (Grounds 4 and 6) do not demonstrate a CPLD receiving BA signals." Dec. 39.

When discussing the obviousness rejection based on Amidi and Dell 2 (Ground 5), we stated "Amidi teaches emulating a smaller memory module by using an address signal, such as an extra row or column line, but does not specifically discuss using a bank address line." Dec. 79; *see id.* at 79–80 (referring to Grounds 4 and 6 for details). However, we additionally stated Dell 2's teaching "provide[s] some evidence of generating [] chip select or rank select signals in response at least in part to a bank address signal." Dec. 81 (referring to our discussion of "bank address limitation in claim 7"). Notably, the "bank address limitation in claim 7" addressed the previously recited "bank address signals of the set of input control signals are received by both the logic element and the register" (R1 App. Br., App'x A 4 (Claims App'x)), not the logic element generating chip-select signals in response to signals (i)–(iv) as claim 1 now recites (PO Response 3).

Even so, we stated "Amidi suggests other types of memory devices or densities can be used to build the four rank memory module" (Dec. 42 (citing Amidi ¶ 71)) and "Dell 2 teaches a technique for using various types of memory

devices or densities other than those in Amidi, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory device. Dell 2, Abstract, claim 1." *Id.; see also id.* at 42–43 (citing Dell 2, Abstract, 2:40–3:5, claim 1, Fig. 1). We also stated "the discussion of Amidi's CPLD receiving bank address signals . . . based on Dell 2's teaching as previously discussed, does provide some evidence of generating [] chip select or rank select signals in response at least in part to *a* bank address signal." *Id.* at 81 (italics added), *quoted in* R1 Comments 10; *see id.* at 94 (stating "Amidi . . . 'at least suggests generating a chip-select signal in response in part to *a* bank address signal'") (emphasis added), *quoted in* R3 Comments 11. These discussions do not address Amidi's and Dell 2 generating chip select signals in response to signals (ii) or "the bank address signal*s*" as now recited.

The previous Decision also states "Dell 2 provides a teaching or suggestion to direct bank address signals to a CPLD, such as Amidi's, in certain situations, such as when the actual and expected dimensions (e.g., the number of banks) of the memory devices differ for navigating to the correct bank within the rank multiplication scheme as suggested by both Amidi (Amidi ¶ 71) and Dell 2 (Dell 2, 2:32–37, 49–51, claim 1)." *Id.* at 81–82 and *see also* 4th Wang Decl. ¶ 26, *cited in* R1 Comments 11. Requester 2 also states Dell 2 discloses the bank address signals of the "logic element" limitation and one skilled in the art would have recognized generating a CAS or chip-select signal in response to a bank address signal in order to ensure the correct bank is addressed. R2 Comments 9–10 (citing 4th Bagherzadeh Decl. ¶ 10[16], which cites Dell 2, 8:29–44).

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[16] Requester 2 provides no paragraph number. For purpose of this decision, we presume Requester 2 is referring to paragraph 10.

Specifically, Dell 2 teaches a logic circuit (e.g., a switch circuit) that performs a remapping function (e.g., 50) of at least one address signal (e.g., A12) to an additional bank address signal (e.g., BA1) at CAS time to ensure the correct *bank* is addressed. Dell 2, 2:32–37, 49–51, 8:20–40, Fig. 1A. Thus, based on Dell 2's teachings or suggestions and what one skilled in the art would have recognized, we agree with Requester 1 (R1 Comments 10–11), Dr. Wang (4th Wang Decl. ¶ 26), Requester 2 (R2 Comments 9–10), and Dr. Bagherzadeh (4th Bagherzadeh Decl. ¶ 10) that one skilled in the art would have recognized using a logic element, like Amidi's CPLD, to generate a control signal in response to a bank address signal for navigating to the correct *bank* during bank expansion (e.g., generate *bank-select* signals in response to bank address signals).

Although this discussion addresses why bank address signals may be received by a CPLD, this reasoning does not sufficiently address why one skilled in the art would have recognized a CPLD, like Amidi's, (e.g., a logic element) generates *chip-select* signals in response to received bank address signals and the other recited signals (i.e., signals (i), (iii), and (iv) recited in claim 1. That is, having a logic element specifically generate "rank-selecting signals . . . in response to" bank address signals in combination with signals (i), (iii), and (iv) as now claim 1 presently recites does not follow from the above teaching to generate signals for *bank* selection. Nor does the current record sufficiently establish that one skilled in the art would have recognized applying Dell 2's bank expansion technique to Amidi's rank expansion process, such that the combination suggests the "logic element" limitation recited in claim 1. Moreover, even assuming, without deciding, one skilled in the art would have recognized to apply such a regime to Amidi's rank expansion process, the teachings would at best suggest

using one stored bank address signal—not bank address signals or signals (ii) required in claim 1—to generate chip-select signals.

The above-discussed teachings are inadequate to suggest generating *chip-select* signals (e.g., rank select signals) in response to both a row address signal and bank address signal*s* as recited in claim 1. *See* 2d Supp. Sechen Decl. ¶¶ 25 (stating "[t]here is no disclosure or suggestion [in Dell 2] of using [a] bank address to generate a control signal, such as a chip-select signal or a CAS signal"), 26 (stating "[t]here is no suggestion to repurpose a bank address signal for rank multiplication purposes."). Thus, in view of the record as it currently stands, we have reconsidered and withdraw our statement in the previous Decision that combining Dell 2's teaching with Amidi "would have predictably yielded" the logic element receiving bank address signals "so that the necessary rank chip select signals discussed in Amidi are produced" (*id.* at 43) as well as any other similar statements.

We additionally referred to "the previous discussion related to Amidi and Dell 2 concerning the bank address limitations and what these references collectively teach." *Id.* at 81; *see also id.* at 82 and R1 Comments 23 (citing Dec. 81–82). For example, we discussed Dell 2 teaches "storing signals for later use, including during a column access procedure[], to ensure the correct bank is addressed." Dec. 59; *see also id.* at 80. As explained above, this teaching in Dell 2 does not teach or suggest sufficiently to one skilled in the art a "logic element" limitation generating *chip-select* signals in response to both a row address signal (i.e., signal (i)) and bank address signal*s* (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Claim 1's "logic element" limitation alternatively recites generating "gated column access strobe (CAS) signals . . . in response at least in part to (i) row address signal, (ii) the bank address signals, and (iii) the chip-select signal of the set of input control signals and (iv) the PLL clock signal." PO Response 3. Amidi's CPLD 604 does not teach or suggest generating a CAS signal. *See* Amidi, Fig. 6A. Instead, CAS signals enter (e.g., CAS) and exit (e.g., rCAS) register 608. *See id.* Granted, Amidi's register 608 receives row address signals (e.g., Add[n-1:0]), bank address signals (e.g., BA[1:0]), and PLL signals (e.g., CLK0, CLK0_N). *See id.* ¶ 50, Fig. 6A. Yet, Amidi does not describe how the rCAS signal is generated. *See id.* Moreover, Amidi does not teach or suggest register 608 receiving chip-select signals (i.e., signal (iv) in claim 1) or operates as a logic element to generate gated CAS signals as recited. *See id.* As such, Amidi does not teach and suggest the "logic element" limitation in claim 1.

Additionally, Dell 2 does not teach or suggest the above missing feature. As explained above, Dell 2 teaches or suggests storing a bank address signal for use with a logic element (e.g., ASIC 24) during CAS time. Dell 2, 8:29–40, 9:32–34. Yet, there is no discussion of generating a CAS signal in response to signals (i) through (iv) as recited in claim 1. In particular, Dell 2 fails to teach or suggest generating a CAS signal in response to a chip-select signal (i.e., signal (iii)). Nor do we find Dr. Wang's testimony persuasive in teaching or suggesting generating a CAS signal in response to a chip-select signal. *See* Dec. 80–81 (citing 3d Wang Decl. ¶¶ 10–16). On the record, we therefore determine Amidi and Dell 2 collectively do not teach or suggest sufficiently to one skilled in the art the "logic element" limitation generating CAS signals in response to both a row address

signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv). *See also* 2d Supp. Sechen Decl. ¶ 26.

Lastly, Requester 1 points out Dr. Sechen's statement in paragraph 26 regarding "the narrower claim dictates that a row address signal, and not a bank address signal, is received by the logic element separate from the signals received by the registers." 2d Supp. Sechen Decl. ¶ 26, *cited in* R1 Comments 11. We agree with Requester 1 that claim 1's "logic element" limitation as currently recited requires the logic element to receive both a row address signal *and* bank address signals. *See* PO Response 3. From this perspective, Dr. Sechen's statement is confusing. *See* R1 Comments 11. Yet, when focusing on the recitation "the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element" in claim 1 (PO Response 3), Dr. Sechen's testimony is consistent with claim 1's recitation requiring the logic element to receive a separate or different row/column address signal from the row/column address signals entering the register. *See* 2d Supp. Sechen Decl. ¶ 26.

Independent claims 15, 28, and 39 each recite a similar "logic element" limitation to claim 1, which generates gated CAS signals or chip-select signals in response to signals (i) through (iv), including both a row address signal and bank address signals. PO Response 11, 18, 23–24. For the above reasons, we determine Amidi's and Dell 2's teachings are inadequate to teach or suggest the "logic element" limitation in these claims.

Upon reconsideration of the record, we withdraw the rejection of claims 1, 15, 28, and 39 and dependent claims 3, 4, 6, 8, 10–14, 18–20, 22, 24, 27, 29, 31,

32, 34–38, 40, 41, 43, 45–50, 120, 122, and 132–136, which variously depend from claims 1, 15, 28, and 39, based on Amidi and Dell 2.

B. Amidi, Dell 2, and JEDEC 21C

The rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C was newly proposed by Requester 1 in its comments. R1 Comments 12–77. The Examiner adopted this proposed rejection. Ex. Deter. 11. Specifically, concerning the "logic element" limitation found in independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 and dependent claim 58, Requester 1 proposes a similar mapping and reasoning for combining Amidi with Dell 2 to teach or suggest this recitation. *See, e.g.,* R1 Comments 23. Requester 1 adds JEDEC 21-C teaches or suggests transmitting PLL clock signals to a CPLD and, and when combined with Amidi, generating its output control signals (e.g., rank-selecting or chip-select signals) in response to a PLL signal for clocking additional devices on a DIMM. *See* R1 Comments 22 (citing JEDEC 21-C, pp. 38–43), 23. In essence, based on JEDEC 21-C's teaching, Requester 1 states one skilled in the art would have known or recognized modifying Amidi so that the clock signals comes Amidi's PLL 606 (e.g., PLL clock signals) rather than memory connector 602 for clocking DIMM devices. *See id.* at 22–23. This modification, in turn, generates chip-select or rank-selecting signals in response to a PLL clock (i.e., signal (iv)) as recited. *See id.*

Yet, JEDEC 21-C's teaching is not relied upon and does not cure the above-noted deficiencies in Amidi and Dell 2—namely the "logic element" limitation generates gated CAS, chip-select or rank-selecting signals in response to

both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv). We refer above for more details.

Accordingly, we withdraw the adopted rejection of claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 based on Amidi, Dell 2, and JEDEC 21-C.

C. Amidi and Dell 184 (Ground 20)

In our May 31, 2016 Decision, claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 (canceled claims omitted) are rejected under 35 U.S.C. § 103 based on Amidi and Dell 184. Dec. 91–93. Independent claims 52, 67, 77, 82, and 87 include similar recitations to the "logic element" limitation in claim 1 that generates rank-selecting or chip-select signals in response to signals (i) through (iv). *Compare* PO Response 27, 33, 36, 38, and 41 *with id.* at 3. Notably, claims 52, 57, 77, 82, and 87 exclude the alternative recitation of generating a gated CAS signal. *Id.* at 27, 33, 36, 38, and 41.

Our rationale for rejecting these claims based on Amidi and Dell 184 was similar to that proposed for Amidi and Dell 2. Specifically, we noted in the opinion

> The teachings in Dell 184 are similar to Dell 2 previously discussed. That is, both references teach and suggest using various types of memory devices or densities, where the memory device is configured with M banks, but the logic circuit receives address and bank address inputs corresponding to N bank memory devices. *Compare* Dell 184, Abstract, 2:48-3:5, claim 1, a[n]d Fig. 1 *with* Dell 2, Abstract, 2:40–65, claim 1, and Fig. 1. Moreover, using the same findings and reasoning as discussed above, combining Dell 184's teaching with Amidi would have predictably yielded Amidi's CPLD receiving various inputs, including bank address signals, to achieve both the

> desired rank and bank expansion. Such a combination would also predictably result in a logic element generating a first number of chip-select or rank-selecting signals in response to a bank address signal . . . .

Id. at 92–93.

Similar to that noted above when addressing Dell 2, Dell 184 in combination with Amidi may provide a reason why bank address signals may be received by a CPLD, but does not sufficiently address why one skilled in the art would have specifically recognized Amidi's CPLD (e.g., a logic element as recited in claim 52) generates *chip-select* or *rank-selecting* signals in response to signals (i)–(iv) as recited in claims 52, 67, 77, 82, and 87. We refer above for more details.

Requester 2 asserts Patent Owner provided no argument related to the patentability of the claims rejected based on Ground 20 and relied upon the arguments presented for Micron and Amidi. *See* R2 Comments 10 (stating "Patent Owner did not provide any individual analysis concerning the patentability of those claims in view of this rejection, but rather relied on its analysis for the rejections under Micron and Amidi."). We disagree.

Patent Owner states "[t]hese amendments [to the claims presented after the previous Decision] distinguish the claims from the combination of Amidi and Dell 184, as discussed above. *See also* Second Supp. Sechen Decl. Section IV." PO Response 56. In "Section IV" of the declaration, Dr. Sechen discusses the similarities between the teachings of Dell 184 and Dell 2 and further articulates how Dell 184 does not use bank address inputs for rank multiplication. *See* 2d Supp. Sechen Decl. ¶¶ 38, 40–42. As such, when stating "as discussed above" (PO Response 56), Patent Owner was referring to the rejection of Amidi and Dell 2 and not Micron and Amidi as argued.

Accordingly, we withdraw the rejection of claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 based on Amidi and Dell 184.

D. Micron and Amidi (Ground 13)

In our previous Decision, we determined claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41–43, 45, 50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 (canceled claims omitted) were obvious over Micron and Amidi. Dec. 93–99. For this rejection, Patent Owner reasserts Amidi does not use both bank address signals and row address signal for rank multiplication or for generating chip-select signals/CAS signals. PO Response 54 (citing 2d Supp. Sechen Decl. ¶¶ 29–30). As to whether one skilled in the art would be motivated to use bank address signals for proper operation of chip select signals, Patent Owner contends "this is a conclusion of fact and not an indication of what a POSITA[17] would recognize." *Id.* at 55 (citing 2d Supp. Sechen Decl. ¶¶ 32–33); *see also id.* at 55–56 (citing 2d Supp. Sechen Decl. ¶¶ 34–35). Patent Owner argues combining Micron and Amidi to arrive at the claimed invention as amended would not be obvious to one skilled in the art. *Id.* at 56. For reasons discussed below, we are persuaded Micron and Amidi do not teach or suggest the newly recited "logic element" limitation in claim 1 or similar independent claims.

At the outset, we address Patent Owner's argument that Dr. Kozyrakis's testimony represents how an expert—not an ordinarily skilled artisan—would have understood Amidi and that Amidi, which does not teach using bank signals to generate chip-select or CAS signals for rank expansion, is representative of what one skilled in the art would have understood. *Id.* at 54–55 (citing 2d Supp. Sechen Decl. ¶¶ 31–32). We agree with Requester 3 that Dr. Kozyrakis's testimony is

[17] "POSITA" stands for a person of ordinary skill in the art.

the references' teachings a logic element generates gated CAS signals or chip-select signals in response to signals (i)–(iv) as recited in claims 1, 15, 28, 39, 52, and 58.

As for Memory Explained, the Examiner stated and we agree that this reference, even when combined with Micron, Amidi, and Olarig, does not teach or suggest generating CAS or chip-select signals in response to bank address signals (i.e., signals (ii)) as well as recited signals (i), (iii), and (iv). RAN 58–69. Requester 3 does not rebut this determination. R3 App. Br. 19 (asserting Micron, Amidi, and Olarig teach these features). In particular, Requester 3 turns to Memory Explained to teach the features recited in dependent claim 56, not the features in independent claim 52. *See* Requester 3's February 13, 2013 Comments 24–25. App'x S.

For the above reasons, we determine the Examiner has not erred in not adopting the proposed rejection of claim 56 (as well as claims 60–63, 80, 81, 85, 86, 90, 91, 109–111, 127, and 131)[21] based on Micron, Amidi, Olarig, and Memory Explained (Ground 22).

V. CONCLUSIONS

We withdraw the following rejections maintained or adopted by the Examiner.

(1) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 120, 122, and 132–136 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2 (Ground 5).

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[21] Despite including only claim 56 in our previous Decision (Dec. 69), Requester 3 appealed the Examiner not adopting the rejection of claim 56 as well as the remaining claims listed above. R3 App. Br. 19–22.

(2) Claims 52, 54, 56, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Amidi and 184 (Ground 20).

(3) Claims 1, 3, 4, 6, 8, 10–15, 18–20, 22, 24, 27–29, 31, 32, 34–41, 43, 45–50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Amidi, Dell 2, and JEDEC 21-C.

(4) Claims 1, 3, 4, 6, 8, 10, 11, 15, 18–20, 22, 24, 27–29, 31, 32, 36–39, 41, 43, 45, 50, 52, 54, 56, 58, 60–63, 67, 69–71, 75, 77, 78, 80–83, 85–88, 90, 91, 109–111, 120, 122, 123, 125–127, and 131–136 are rejected under 35 U.S.C. § 103 based on Micron and Amidi (Ground 13).

(5) Claims 52, 54, 67, 69–71, 77, 78, 82, 83, 87, and 88 are rejected under 35 U.S.C. § 103 based on Micron, Amidi, and Olarig (Ground 21).

We further affirm the Examiner's decision not to adopt the rejection of certain claims based on Micron, Amidi, Dell 2, and JEDEC 79C (Ground 19) or Micron, Amidi, Olarig, and Memory Explained (Ground 22), previously not reached.

Based on our previous Decision, we note the following rejections are affirmed.

(1) Claim 9 and 33 is rejected under 35 U.S.C. § 102 based on Amidi. Dec. 11, 13, 23.

(2) Claims 2, 5, 7, 9, 21, 23, 30, 33, 57, and 119 are rejected under 35 U.S.C. § 103 based on (a) Amidi or (b) Amidi and JEDEC. Dec. 12–13, 39, 57.

(3) Claims 2, 5, 7, 9, 21, 23, 26, 30, and 33 are rejected under 35 U.S.C. § 103 based on Amidi and Dell 2. Dec. 12–13, 43, 60.

(4) Claims 7, 9, 21, 26, 33, and 57 are rejected under 35 U.S.C. § 103 based on Micron and Amidi. Dec. 12–13, 66–67.

(5) Claim 9 is rejected based on (a) Dell 1[22] and JEDEC under 35 U.S.C. § 103 (RAN 13, 36–39) (Ground 9), (b) Wong[23] and JEDEC under 35 U.S.C. § 103 (RAN 13, 41–43) (Ground 11), and (c) Micron and Connolly[24] under 35 U.S.C. § 103 (RAN 13, 44–47) (Ground 12). Dec. 12–13.

We also note the Examiner's decision not to adopt the proposed rejection of claims 16 and 17 based on Amidi and Dell 2 remains affirmed and we do not reach the propriety of the non-adopted rejection of claim 119 under Ground 5. Dec. 82–83.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

37 C.F.R. § 41.77(f)

[22] U.S. Patent No. 5,926,827 (issued July 20, 1999) (Dell 1).
[23] U.S. Patent No. 6,414,868 (issued July 2, 2002) (Wong).
[24] U.S. Patent No. 5,745,914 (issued April 28, 1998) (Connolly).

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Patent 7,619,912 B2

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